



Fabrication of SiGe/Ge nanostructures by three-dimensional Ge condensation of sputtered SiGe on SiO₂/Si substrate



Guangyang Lin^{a, b}, Haiyang Hong^b, Jie Zhang^a, Yuying Zhang^c, Peng Cui^a, Jianyuan Wang^b, Songyan Chen^b, Yong Zhao^c, Chaoying Ni^c, Cheng Li^{b, *}, Yuping Zeng^{a, **}

^a Department of Electrical and Computer Engineering, University of Delaware, Newark, DE, 19716, USA

^b Key Laboratory of Low Dimensional Condensed Matter Physics (Department of Education of Fujian Province), Department of Physics, Xiamen University, Xiamen, Fujian, 361005, People's Republic of China

^c Department of Materials Science and Engineering, University of Delaware, Newark, DE, 19716, USA

ARTICLE INFO

Article history:

Received 16 April 2020

Received in revised form

1 October 2020

Accepted 19 October 2020

Available online 20 October 2020

Keywords:

Three-dimensional Ge condensation

Heterojunction

Nanostructure

Schottky barrier height

ABSTRACT

In this work, three-dimensional (3D) Ge condensation of sputtered “Si/SiGe” nanostructures on SiO₂/Si substrate was investigated. Through varying the width of sputtered Si/SiGe structures from 50 μm to 400 nm, the Ge content of fabricated SiGe structures can be modulated from 0.49 to 1.0 after 3D Ge condensation. By further constructing a width modified nanowire (NW) with adjacent widths of 800 nm and 400 nm before 3D Ge condensation, a Si_{0.33}Ge_{0.67}/Ge heterostructure NW was fabricated after 3D Ge condensation. Due to inter-diffusion of Si and Ge atoms, a ~2-μm-long region with gradually varied Ge content from ~0.67 to 1.0 is formed between Si_{0.33}Ge_{0.67} and Ge. The low Schottky barrier height (0.29 eV) of Ge NW/metal contact and good conductivity of the Ge NW suggest that the 3D Ge condensation technique is very promising for fabrication of scalable and low-cost SiGe or Ge nano-electronic/photonic devices.

© 2020 Elsevier B.V. All rights reserved.

1. Introduction

Germanium (Ge) has been considered as one of the most promising candidate materials for silicon (Si) based electronic and optoelectronic devices. The driving force for integration of Ge with Si includes its high carrier mobility, large light absorption coefficient at telecom wavelength (~1550 nm), quasi-direct band structure and compatibility with Si processing technology. To date, the application of Ge-on-Si material in metal-oxide-semiconductor field-effect-transistor (MOSFET) [1,2], photodetector [3,4] and even light emitting device [5,6] have been widely investigated. With “on-insulator” structure, both the electronic and optoelectronic performance of Ge-based devices can be further improved. The isolation of Ge with substrate is beneficial to reduce parasitic capacitance and leakage current. Additionally, light resonance and confinement can be realized due to large difference of refractive

index between Ge and the insulator. Many techniques have been developed to fabricate Ge-on-insulator (GOI) substrate such as wafer bonding [7], smart-cut [8], solid-phase crystallization [9,10], and Ge condensation [11,12]. Through cyclic oxidation and annealing of SiGe-on-insulator (SGOI) material at high temperature (≥900 °C), Ge condensation can be used to fabricate high quality GOI materials with thickness of <50 nm. Although many studies have contributed to Ge condensation [13–16], previous investigations mainly focus on the Ge condensation effect of single crystal SGOI sample with planar structure. Few studies have reported on Ge condensation effect of SGOI with nanostructures [17,18], especially for amorphous SGOI, which can be fabricated by low-cost methods. Recently, we have carried out 3D Ge condensation of single crystal SGOI nanowires (NWs) [19]. It is found that the final Ge content of SiGe NW can be modulated by varying the initial width of SGOI NW. However, the 3D Ge condensation effect of amorphous SGOI nanostructures needs to be further investigated.

In this work, 3D Ge condensation of sputtered “Si/SiGe” nanostructures on SiO₂/Si substrate was investigated. By varying the width of sputtered Si/SiGe structures from 50 μm to 400 nm, the Ge

* Corresponding author.

** Corresponding author.

E-mail addresses: gylin@udel.edu (G. Lin), lich@xmu.edu.cn (C. Li), yzeng@udel.edu (Y. Zeng).

content in SiGe structures was modulated from 0.49 to 1.0 after 3D Ge condensation. After 3D Ge condensation of a width modified NW with adjacent widths of 800 nm and 400 nm, a lateral $\text{Si}_{0.33}\text{Ge}_{0.67}/\text{Ge}$ heterostructure NW was further fabricated. The low Schottky barrier height (0.29 eV) of Ge NW/metal contact and good conductivity of the Ge NW manifest that the fabricated nanostructure has a very good potential for nano-electronic/photonic devices. The proposed 3D Ge condensation of technique is very promising for fabrication of scalable and low-cost SiGe or Ge nanostructures.

2. Material and methods

Sample fabrication was based on a SiO_2/Si substrate. The 300-nm-thick SiO_2 was obtained by thermal oxidation of a Si (100) wafer. The substrate was firstly degreased by ultrasonic bath of acetone, ethanol and de-ionized (DI) water, then blown dried with nitrogen. Next, a 71-nm-thick $\text{Si}_{0.77}\text{Ge}_{0.23}$ layer and 5-nm-thick Si cap layer were successively grown on SiO_2/Si substrate via direct current (DC) magnetron sputtering. The SiGe layer was obtained through co-sputtering of Si and Ge targets under 0.4 Pa with a DC power of 104 W and 9 W, respectively. The structure diagram of the as-grown sample is displayed in Fig. 1(a). Fig. 1(b) shows the depth profiles of Si, Ge and O atoms for the as-grown sample taken from Auger electron spectroscopy (AES, Physical Electronics PHI 660). As can be seen, a uniform SiGe layer with an average Ge content of 0.23 was formed on SiO_2 . Fig. 1(c) exhibits the X-ray reflection (XRR, PANalytical X'Pert PRO) curve (black curve) of the as-grown sample. From fitting results of the XRR curve (red curve) with 'Si cap/SiGe/ SiO_2/Si substrate' structure, the thicknesses of SiGe and Si cap layers were verified. The observation of multiple fringe peaks in the XRR curve indicates that the surface and interfaces in the structure are rather flat [20]. To perform 3D Ge condensation process, the deposited material was then patterned into NW structures by e-beam lithography (EBL) and reactive ion etch (RIE) techniques. Fig. 1(d) presents the structure diagram of a patterned NW structure. To fully isolated the NW, part of the SiO_2/Si substrate was also etched. The NW with length of 45 μm is fixed between two

$50 \times 50 \mu\text{m}^2$ pads. The NW width in different patterns varies from 400 nm to 800 nm. The sample was then loaded into a 2-inch furnace to carry out 3D Ge condensation process. Fig. 1(e) displays the key steps of the 3D condensation process. The whole condensation process was conducted through C_1 , C_2 and C_3 steps at 900 °C. Each condensation step includes 10 cycles of 10-min oxidation and subsequent 10-min annealing. The oxidation and annealing process were performed in dry O_2 with purity of 99.999% and N_2 with purity of 99.999%, respectively. The flow rate of O_2 and N_2 was 1.2 L/min. Sample evolution after each Ge condensation step was characterized by Raman spectra, which was excited by a 488-nm laser and collected by WITec alpha300 confocal micro-Raman system.

3. Results and discussion

Fig. 2(a)–2(d) display the evolution of Raman spectra for SiGe pad, SiGe NW with initial width of 800 nm, 600 nm and 400 nm before Ge condensation process (black curve), after C_1 (red curve), C_2 (green curve) and C_3 (blue curve) Ge condensation steps, respectively. Four Raman modes are observed in the spectra: Ge–Ge mode ($250\text{--}300 \text{ cm}^{-1}$), Si–Ge mode ($\sim 400 \text{ cm}^{-1}$) and Si–Si mode ($450\text{--}500 \text{ cm}^{-1}$) from SiGe, Si–Si mode ($\sim 520.6 \text{ cm}^{-1}$) from Si substrate. The observation of well-shaped Si–Si, Si–Ge and Ge–Ge modes of SiGe implies formation of SiGe nano- or micro-crystal. As can be seen, from C_1 to C_3 Ge condensation steps, the intensity ratio between Ge–Ge mode and Si–Si mode of SiGe in all structures gradually becomes larger manifesting continuously enrichment of Ge. Under the same Ge condensation process, the Raman spectra from structures with different widths vary greatly. As the width of SiGe structure decreases from 50 μm to 400 nm, the intensity ratio between Si–Si mode and Ge–Ge mode of SiGe reduces suggesting that higher Ge content is achieved in narrower SiGe structure. For SiGe NW with initial width of 400 nm, both Si–Ge and Si–Si modes of SiGe disappear after C_3 Ge condensation step manifesting acquisition of pure Ge NW.

Based on the peak positions of Si–Si and Si–Ge modes of SiGe, the calculation of Ge content (x) and strain (ϵ_{ij}) in $\text{Si}_{1-x}\text{Ge}_x$ with

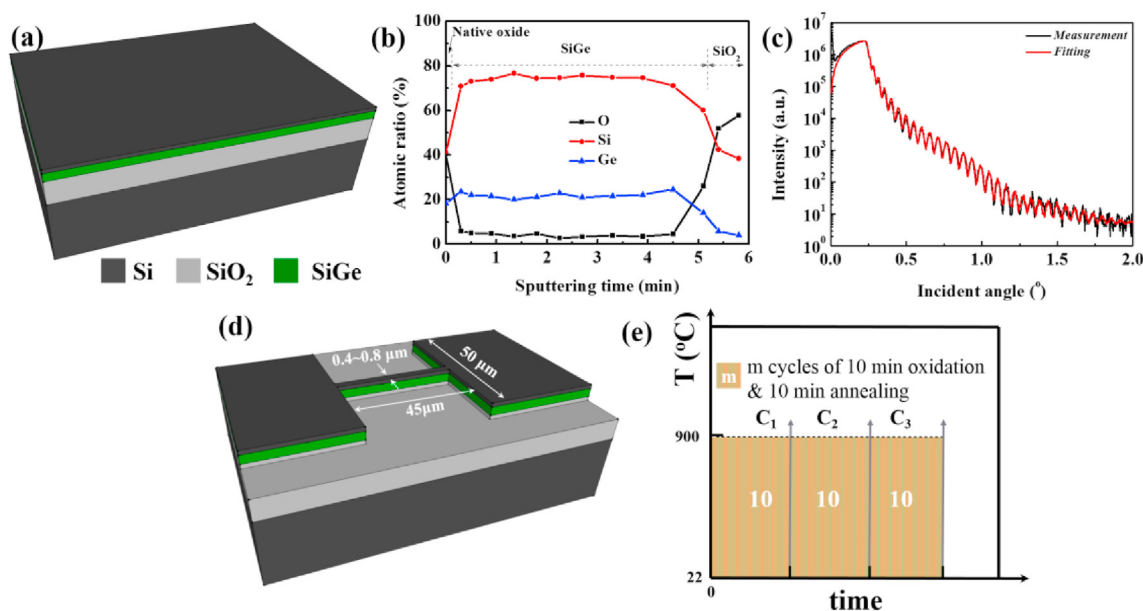


Fig. 1. (a) Structure diagram of the sputtered "Si/SiGe" structure on SiO_2/Si substrate for 3D Ge condensation; (b) Si, Ge and O depth profiles of the sputtered sample measured from AES; (c) XRR curve of the sputtered sample and related fitting result; (d) structure diagram of the designed NW structure before 3D Ge condensation; (e) key steps of 3D Ge condensation process.

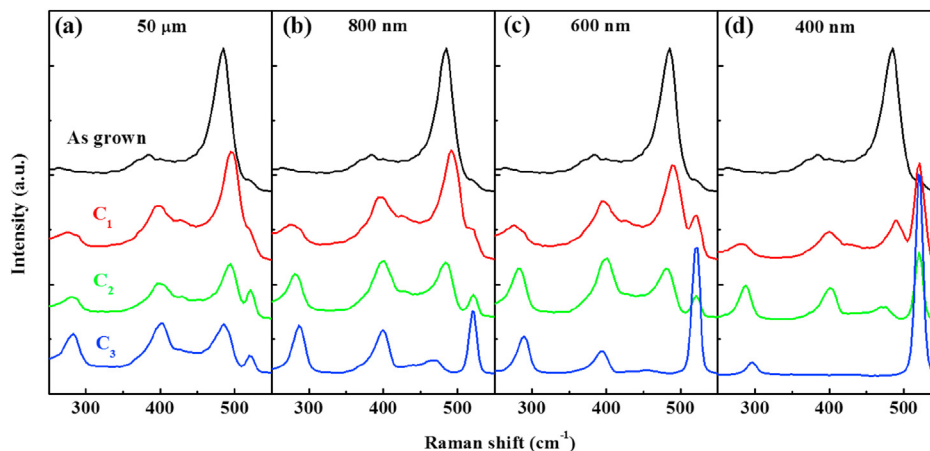


Fig. 2. Raman spectra of (a) SiGe pad with dimension of $50 \times 50 \mu\text{m}^2$, SiGe NW with width of (b) 800 nm, (c) 600 nm and (d) 400 nm before Ge condensation process (black curve) and after C₁ (red curve), C₂ (green curve) and C₃ (blue curve) Ge condensation steps, respectively. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

$x < 0.5$ has been investigated [21–23]:

$$\begin{aligned} \omega_{\text{Si-Si}}(\text{cm}^{-1}) &= 520.6 - 62x - 815\epsilon_{\parallel} \\ \omega_{\text{Si-Ge}}(\text{cm}^{-1}) &= 400.5 + 14.2x - 575\epsilon_{\parallel} \end{aligned} \quad (1)$$

With the integral intensity ratio between Ge–Ge ($I_{\text{Ge-Ge}}$) and Si–Ge ($I_{\text{Si-Ge}}$) modes of SiGe, the Ge content in $\text{Si}_{1-x}\text{Ge}_x$ with $x > 0.5$ can be evaluated by the following equation instead [23–25]:

$$\frac{I_{\text{Ge-Ge}}}{I_{\text{Si-Ge}}} = \frac{Bx}{2(1-x)} \quad (2)$$

where B is the coefficient related to Raman setup. For our Raman system, B is determined to be 1 according to our previous studies [25]. The solid lines in Fig. 3(a) display the evolution of Ge content in SiGe structures after C₁–C₃ Ge condensation steps. The detailed x values are summarized in Table 1. For SiGe with initial width of 50 μm , 800 nm, 600 nm and 400 nm, the Ge content after C₁ step is 0.25, 0.29, 0.31 and 0.37, respectively; after C₂ step, the Ge content increases to 0.29, 0.44, 0.48 and 0.67, respectively; after C₃ step, the Ge content enriches to 0.49, 0.68, 0.75 and 1.0, respectively. The evolutionary trend of Ge content during 3D Ge condensation of amorphous SiGe is similar to that during 3D Ge condensation of single crystal SiGe [19]. As Ge condensation process proceeds, higher Ge content is achieved in narrower SiGe structure, and the Ge content difference in different structures becomes larger.

The dash lines in Fig. 3(a) show the strain evolution in SiGe

Table 1

Evolution of Ge content (x) and strain (ϵ_{\parallel}) in SiGe wires with different widths after Ge condensation steps of C₁–C₃.

SiGe width	C ₁		C ₂		C ₃	
	x	ϵ_{\parallel} (%)	x	ϵ_{\parallel} (%)	x	ϵ_{\parallel} (%)
50 μm	0.25	1.42	0.29	1.27	0.49	1.10
800 nm	0.29	1.37	0.44	1.13	0.68	0.90
600 nm	0.31	1.26	0.48	0.94	0.75	0.72
400 nm	0.37	0.97	0.67	0.78	1.0	0.56

structures after C₁–C₃ Ge condensation steps. Detailed ϵ_{\parallel} values are listed in Table 1. For as-deposited film, a large tensile strain of 2.26% is detected in the as-deposited film probably due to porous structure and grain boundary relaxation [26]. As Ge condensation proceeds, the tensile strain in SiGe gradually relaxes. The change of strain may be related to the change of crystal quality and thermal strain between SiGe and SiO₂. The larger thermal expansion coefficient (TEC) of SiGe ($2.6\text{--}8.5 \times 10^{-6} \text{K}^{-1}$) [27,28] than that of SiO₂ ($0.5 \times 10^{-6} \text{K}^{-1}$) [29] would induce an extra tensile strain in the SiGe film during sample cooling from 900 °C to room temperature. However, as the Ge content gradually enriches, the crystal quality improves. The film structure becomes denser leading to gradual relaxation of the tensile strain. For the pure Ge, a tensile strain of 0.56% is detected. The improved crystal quality and tensile strain is beneficial to enhance the carrier mobility [30,31].

To examine the crystal quality and orientation, the cross-section images of 50- μm -wide SiGe after C₃ condensation step were taken

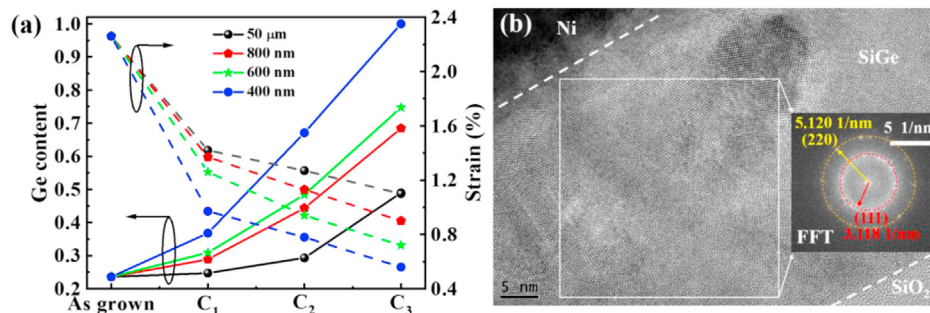


Fig. 3. Evolution of (a) Ge content (solid) and strain (dash) in SiGe pad and SiGe NWs with initial width of 400–800 nm after C₁–C₃ 3D Ge condensation steps. (b) Cross-section TEM image of SiGe with initial width of 50 μm after C₃ Ge condensation step. The inset shows the FFT of the square area.

by transmission electron microscope (TEM, FEI Tecnai G² F20 S-Twin), as shown in Fig. 3(b). Clear nanocrystals with different orientations can be observed in the SiGe film suggesting polycrystalline structure of the film. The inset of Fig. 3(b) shows the Fast Fourier Transform (FFT) of the square area. Some diffraction dots located at two concentric circles are observed. The radiuses of the outer and inner circles are measured as $R_1 = 5.120 \text{ nm}^{-1}$ and $R_2 = 3.118 \text{ nm}^{-1}$, respectively. From $R_1^2 : R_2^2 \approx 8 : 3$, nanocrystals along (220) and (111) facets can be confirmed.

From the above results, it is inferred that by varying the widths of adjacent regions in SiGe NW, SiGe or SiGe/Ge heterostructure NWs can be feasibly fabricated after same 3D Ge condensation process. To verify this conjecture, we further carried out 3D Ge condensation process of a width modified SiGe NW. The NW with total length of 45 μm is fixed between two $50 \times 50 \mu\text{m}^2$ pads. With different width along the longitudinal direction, the NW can be divided into three parts: the two adjacent to the pads has a length of 20 μm and a width of 800 nm; the one at middle has a length of 5 μm and width of 400 nm. The structure was then subjected to C₁–C₃ 3D Ge condensation process as displayed in Fig. 1(e).

Fig. 4(a) displays the mapping of Raman integral intensity of Si–Ge mode ($340\text{--}410 \text{ cm}^{-1}$) for the width modified SiGe NW after C₃ 3D Ge condensation step. The spatial resolution of Raman mapping is 250 nm. As can be seen, the intensity from the NW region with initial width of 800 nm is strong, while the signal from the NW region with initial width of 400 nm can be barely detected. Fig. 4(b) shows the mapping of Raman peak position of Ge–Ge mode for the width modified SiGe NW after C₃ Ge condensation step. The appearing of Ge–Ge mode and absence of Si–Ge mode in the NW region with initial width of 400 nm suggests formation of pure Ge. The frequency of Ge–Ge mode in NW region with initial width of 400 nm ($\sim 295.8 \text{ cm}^{-1}$) is much higher than that in NW region with initial width of 800 nm (286.1 cm^{-1}) manifesting formation of SiGe/Ge heterojunction NW. To further investigate the

uniformity of the 3D Ge condensation process, lateral distribution of Ge content and strain along the heterojunction NW (in region I of Fig. 4(b)) is analyzed using equations [1,2]. Fig. 4(c) shows the distribution of Ge content (black) and strain (red) along the NW. Around 1.0–1.2% tensile strain is observed in the detected region. As the initial width of SiGe NW decreases from 800 to 400 nm, the Ge content after 3D Ge condensation process gradually increases from ~ 0.67 to 1.0 within the length of $\sim 2 \mu\text{m}$. The result suggests that a SiGe/Ge heterojunction NW with gradually changed Ge content is obtained, which is beneficial for carrier confinement in the Ge region through tailoring the band profile [32]. The formation of NW region with gradually changed Ge content is due to interdiffusion of Si and Ge atoms during Ge condensation process between adjacent NW regions with different initial widths.

Fig. 4(d) shows the surface morphology of the Ge/SiGe NW taken by atomic force microscope (AFM, Bruker Multimode 8). The surface SiO₂ on NW generated during Ge condensation process was not removed. The line profiles along the NW (blue) and substrate (black) are compared in Fig. 4(e). The substrate is rather flat. As the NW width decreases, a gradual increase of $\sim 16 \text{ nm}$ in height within a length of $\sim 2 \mu\text{m}$ is observed. As discussed in Fig. 4(c), as the initial NW width decreases from 800 to 400 nm, the Ge content after 3D Ge condensation process gradually increases from ~ 0.67 to 1.0. It is reported that the oxidation rate of SiGe increases with the Ge content [33]. Hence, the increase of surface height of the NW is due to generation of thicker SiO₂ during 3D Ge condensation process in higher Ge content region.

To characterize the electrical property of the Ge NW fabricated by 3D Ge condensation of a sputtered SiGe NW, a metal-semiconductor-metal (MSM) structure was fabricated with 30-nm Ni/50-nm Au as contact metal. The optical image of the fabricated Ge MSM structure is displayed in Fig. 5(a). The width of metal/Ge NW contacts and the spacing between the two contacts are both 1 μm . Fig. 5(b) shows the room temperature *IV* curves of the MSM structure in semi-log (black curve) and linear (red curve) scales

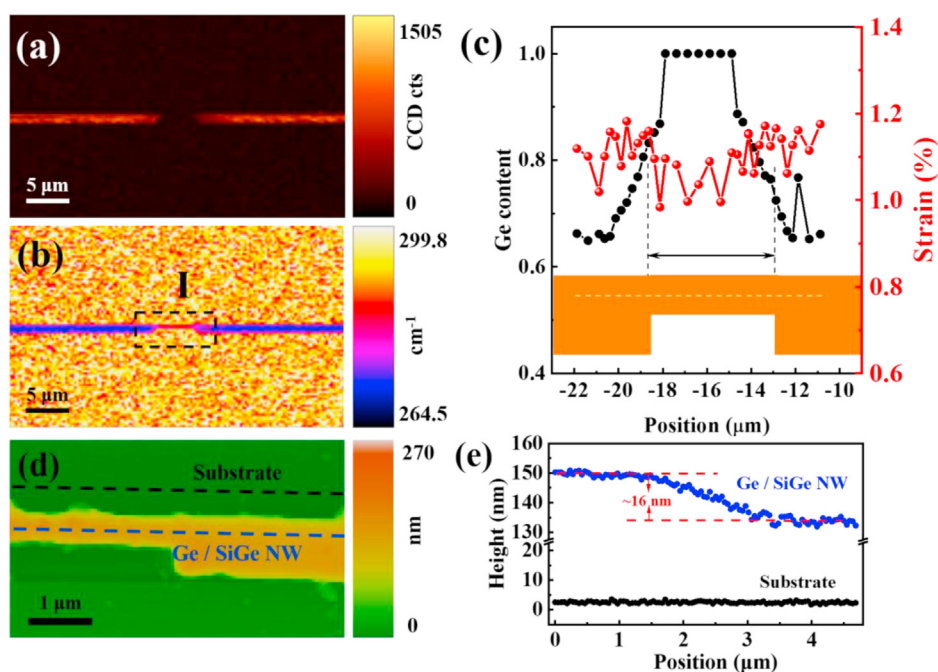


Fig. 4. (a) Mapping of Raman integral intensity of Si–Ge mode ($340\text{--}410 \text{ cm}^{-1}$) and (b) mapping of Raman peak position of Ge–Ge mode for a width modified SiGe NW after C₃ 3D Ge condensation step. (c) Calculated Ge content distribution along the SiGe/Ge heterojunction NW in region I of Fig. 4(b). (d) AFM image of the width modified SiGe NW after C₃ 3D Ge condensation step. (e) AFM line profiles along the NW (blue) and substrate (black) extracted from Fig. 4(d). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

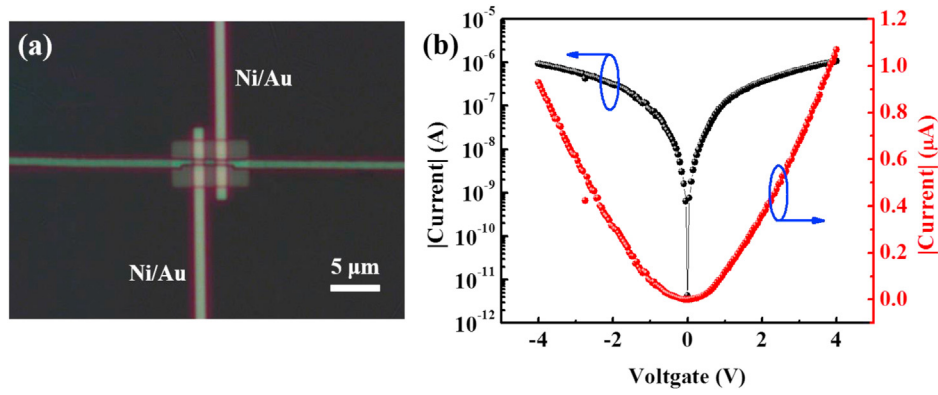


Fig. 5. (a) Optical image of Ge NW MSM structure and (b) corresponding IV curves in semi-log (black curve) and linear (red curve) scales. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

under dark, respectively. The dependence of current (I) on applied voltage (V) is slightly nonlinear suggesting existence of a Schottky barrier between Ge NW and Ni.

For a Schottky contact, the dependence of I on V can be analyzed by the following equation [34]:

$$I = I_0 \exp\left(\frac{qV}{nkT}\right) \left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \quad (3)$$

where $I_0 = A^*ST^2 \exp\left(-\frac{q\phi}{kT}\right)$ is the saturation current, A^* is the Richardson constant, k is the Boltzmann constant, T is the absolute temperature, q is the electronic charge, S is the contact area, ϕ is Schottky barrier height (SBH) of metal/semiconductor contact, and n is the ideality factor. For MSM structure, the IV curves can be characterized by equation [3] under reverse bias. Under $V \leq -0.5$ V and $T \leq 370$ K, equation [3] can be simplified as [35]:

$$I \exp\left(\frac{qV}{kT}\right) = I_0 \exp\left(\frac{qV}{nkT}\right). \quad (4)$$

It should be noted that absolute values of reverse current I have been substituted into equation [4] to facilitate subsequent analysis. By linear fitting of $\ln[I \exp(qV/kT)] \sim V$ curve, n and I_0 can be obtained from the slope (q/nkT) and intercept ($\ln I_0$), respectively. Through further measurement of temperature dependent IV curves, ϕ can be extracted by:

$$\phi = \frac{k}{q} \frac{d[\ln(I_0/T^2)]}{d(1/T)} \approx 0.2 \frac{d[\log(I_0/T^2)]}{d(1000/T)}. \quad (5)$$

Fig. 6(a) shows the IV curves of the Ge NW MSM structure at 25–50 °C under 0–2.0 V. The dependence of $\ln[I \exp(qV/kT)]$ on V and related linear fitting results under different temperatures are

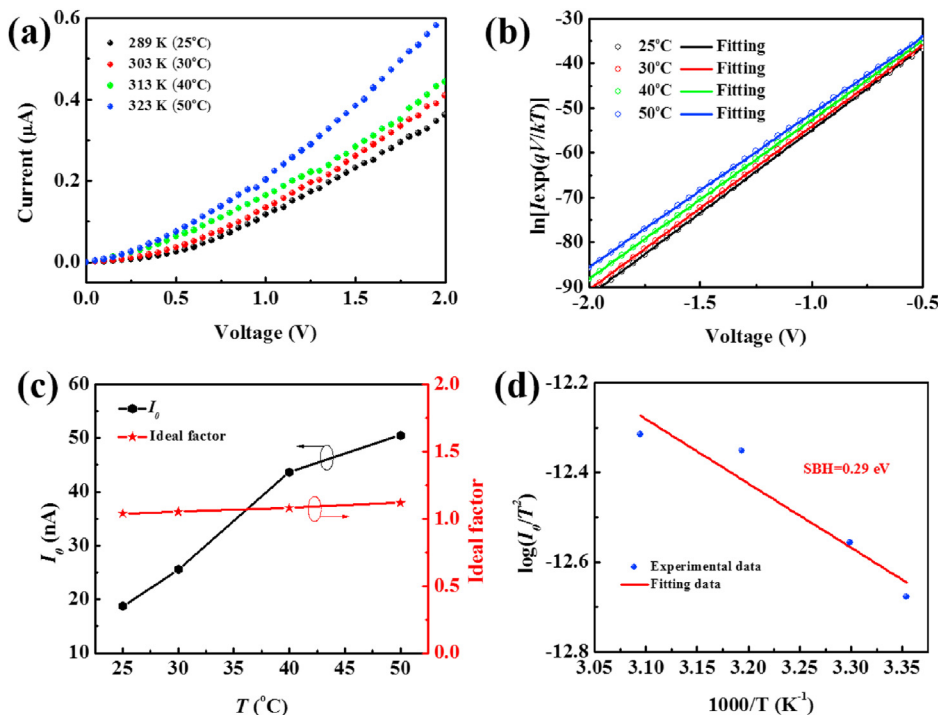


Fig. 6. (a) Forward IV curve of fabricated Ge NW MSM structure under 289–323 K; (b) dependence of $\ln[I \exp(qV/kT)]$ on V under 289–323 K; (c) extracted dependence of I_0 and n on sample temperature; (d) $\log(I_0/T^2)$ as a function of $1000/T$, from which a SBH of 0.29 eV is extracted.

displayed in Fig. 6(b). From the slope and intercept of the $\ln [I_{\text{exp}}(qV/kT)]-V$ linear fitting curve, the n and I_0 values under different T can be calculated. Fig. 6(c) shows the dependences of n and I_0 on T . As T elevates from 25 to 50 °C, I_0 increases from ~20 nA to ~50 nA due to increase of thermal activated carriers; n slightly increases from 1.04 to 1.12 suggesting that the current is dominated by a diffusion mechanism [36] at 25–50 °C. Fig. 6(d) shows the dependence of $\log(I_0/T^2)$ on $(1000/T)$ and related linear fitting result. Based on equation [5], a ϕ of 0.29 eV can be calculated from the slope. It has been reported that the charge neutrality level (CNL) of Ge is pinned at ~0.1 eV above the top of valance band [37]. The small ϕ between Ge NW and Ni implies that the Ge NW is unintentionally p doped induced by vacancies in Ge. The extracted ϕ is slightly higher than that of bulk p -Ge/metal contact (~0.1 eV) due to quantum confinement effect in Ge NW, which induces an additional hole barrier.

The current of Ge NW MSM structure at ± 1 V is 0.1 μA corresponding to a current density of ~25 A/cm^2 . The current density is comparable with that of bulk Ge/metal ohmic contact [38] manifesting good conductivity of the Ge NW. The good conductivity can be attributed to large surface to volume ratio of NW and low SBH between Ni and Ge NW. The good conductivity of the Ge NW suggests the potential application in low-cost nano-electronic, such as transistors and biosensors [39]. The SiGe/Ge heterojunction NW, which can effectively confine the carriers in Ge region and may provide carrier multiplication mechanisms [40], can be potentially used for nano-photonic devices, such as solar cells [41].

4. Conclusions

In summary, 3D Ge condensation of sputtered “Si/SiGe” nanostructures on SiO_2/Si substrate was investigated. Through varying the width of “5-nm Si/71-nm $\text{Si}_{0.77}\text{Ge}_{0.23}$ layer” wires on SiO_2/Si substrate from 50 μm to 400 nm, the Ge content of fabricated SiGe-on-insulator (SGOI) can be modulated from 0.49 to 1.0 after 3D Ge condensation. By further modifying the widths of the adjacent regions of a “Si/SiGe” NW from 800 to 400 nm before 3D Ge condensation, a $\text{Si}_{0.33}\text{Ge}_{0.67}/\text{Ge}$ heterostructure NW was fabricated after 3D Ge condensation. Due to inter-diffusion of Si and Ge atoms, a ~2- μm -long region with gradually increased Ge content from ~0.67 to 1.0 was formed between $\text{Si}_{0.33}\text{Ge}_{0.67}$ and Ge. A Ni/Ge NW/Ni MSM structure was fabricated to further characterize the electrical property of the Ge NW. The achievement of low Schottky barrier height of Ge NW/Ni contact and good conductivity of the Ge NW suggest that the 3D Ge condensation method is very promising for fabrication of scalable and low-cost SiGe or Ge nanostructures.

CRedit authorship contribution statement

Guangyang Lin: Conceptualization, Investigation, Writing - original draft. **Haiyang Hong:** Investigation, Validation. **Jie Zhang:** Methodology, Visualization. **Yuying Zhang:** Formal analysis. **Peng Cui:** Methodology. **Jianyuan Wang:** Resources. **Songyan Chen:** Methodology. **Yong Zhao:** Formal analysis. **Chaoying Ni:** Formal analysis. **Cheng Li:** Supervision, Funding acquisition, Writing - review & editing. **Yuping Zeng:** Supervision, Data curation, Writing - review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

This work is supported by National Key R&D Program of China under grant No. 2018YFB2200103, National Natural Science Foundation of China under grant No. 61474094 and 61176092. This work is also partially supported by the start-up funding from University of Delaware. This work is also partially supported by Air Force Office of Scientific Research under Grant No. FA9550-19-1-0297.

References

- [1] H. Liu, G. Han, Y. Liu, Y. Hao, High mobility Ge pMOSFETs with ZrO_2 dielectric: impacts of post annealing, *Nanoscale Research Letters* 14 (1) (2019) 202.
- [2] L. Hutin, C.L. Royer, J. Damlencourt, J. Hartmann, H. Grampeix, V. Mazzocchi, C. Tabone, B. Previtali, A. Pouydebasque, M. Vinet, O. Faynot, GeOI pMOSFETs scaled down to 30-nm gate length with record off-state current, *IEEE Electron. Device Lett.* 31 (3) (2010) 234–236.
- [3] Y. Salamin, P. Ma, B. Baeuerle, A. Emboras, Y. Fedoryshyn, W. Heni, B. Cheng, A. Josten, J. Leuthold, 100 GHz plasmonic photodetector, *ACS Photonics* 5 (8) (2018) 3291–3297.
- [4] G. Lin, D. Liang, C. Yu, H. Hong, Y. Mao, C. Li, S. Chen, Broadband 400–2400 nm Ge heterostructure nanowire photodetector fabricated by three-dimensional Ge condensation technique, *Optic Express* 27 (22) (2019) 32801–32809.
- [5] J. Liu, X. Sun, D. Pan, X. Wang, L.C. Kimerling, T.L. Koch, J. Michel, Tensile-strained, n-type Ge as a gain medium for monolithic laser integration on Si, *Optic Express* 15 (18) (2007) 11272–11277.
- [6] G. Lin, X. Yi, C. Li, N. Chen, L. Zhang, S. Chen, W. Huang, J. Wang, X. Xiong, J. Sun, Strong room temperature electroluminescence from lateral p-SiGe/i-Ge/n-SiGe heterojunction diodes on silicon-on-insulator substrate, *Appl. Phys. Lett.* 109 (14) (2016) 141104.
- [7] J.R. Jain, D.-S. Ly-Gagnon, K.C. Balram, J.S. White, M.L. Brongersma, D.A.B. Miller, R.T. Howe, Tensile-strained germanium-on-insulator substrate fabrication for silicon-compatible optoelectronics, *Opt. Mater. Express* 1 (6) (2011) 1121–1126.
- [8] C. Deguet, C. Morales, J. Dechamp, J.M. Hartmann, A.M. Charvet, H. Moriceau, F. Chieux, A. Beaumont, L. Clavelier, V. Loup, N. Kernevez, G. Raskin, C. Richtarch, F. Allibert, F. Letertre, C. Mazure, Germanium-on-insulator (GeOI) structures realized by the Smart Cut/spl trade/technology. *IEEE International SOI Conference*, IEEE Cat. No.04CH37573, 2004, pp. 96–97, 2004.
- [9] R. Yoshimine, K. Moto, T. Suemasu, K. Toko, Advanced solid-phase crystallization for high-hole mobility ($450 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) Ge thin film on insulator, *APEX* 11 (3) (2018), 031302.
- [10] D. Takahara, R. Yoshimine, T. Suemasu, K. Toko, High-hole mobility $\text{Si}_{1-x}\text{Ge}_x$ ($0.1 \leq x \leq 1$) on an insulator formed by advanced solid-phase crystallization, *J. Alloys Compd.* 766 (2018) 417–420.
- [11] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, S.-i. Takagi, Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique, *Appl. Phys. Lett.* 83 (17) (2003) 3516–3518.
- [12] N. Hirashita, Y. Moriyama, S. Nakaharai, T. Irisawa, N. Sugiyama, S.-i. Takagi, Deformation induced holes in Ge-rich SiGe-on-Insulator and Ge-on-Insulator substrates fabricated by Ge condensation process, *APEX* 1 (2008) 101401.
- [13] S. Nakaharai, T. Tezuka, N. Hirashita, E. Toyoda, Y. Moriyama, N. Sugiyama, S. Takagi, Formation process of high-purity Ge-on-insulator layers by Ge-condensation technique, *J. Appl. Phys.* 105 (2) (2009), 024515.
- [14] G. Lin, X. Lan, N. Chen, C. Li, D. Huang, S. Chen, W. Huang, J. Xu, H. Lai, Strain evolution of SiGe-on-insulator fabricated by germanium condensation method with over-oxidation, *Mater. Sci. Semicond. Process.* 56 (2016) 282–286.
- [15] G. Lin, D. Liang, J. Wang, C. Yu, C. Li, S. Chen, W. Huang, J. Wang, J. Xu, Strain evolution in SiGe-on-insulator fabricated by a modified germanium condensation technique with gradually reduced condensation temperature, *Mater. Sci. Semicond. Process.* 97 (2019) 56–61.
- [16] T. David, A. Benkouider, J.-N. Aqua, M. Cabie, L. Favre, T. Neisius, M. Abbarchi, M. Naffouti, A. Ronda, K. Liu, I. Berbezier, Kinetics and energetics of Ge condensation in SiGe oxidation, *J. Phys. Chem. C* 119 (43) (2015) 24606–24613.
- [17] L. Ye, Q. Cai, B. Xu, Z. Di, M. Zhang, J. Yang, High sensitivity biosensors based on germanium nanowires fabricated by Ge condensation technique, *Mater. Lett.* 172 (2016) 142–145.
- [18] M. Naffouti, T. David, A. Benkouider, L. Favre, M. Cabie, A. Ronda, I. Berbezier, M. Abbarchi, Fabrication of core-shell nanostructures via silicon on insulator dewetting and germanium condensation: towards a strain tuning method for SiGe-based heterostructures in a three-dimensional geometry, *Nanotechnology* 27 (30) (2016) 305602.
- [19] G. Lin, D. Liang, C. Yu, H. Hong, Y. Mao, C. Li, S. Chen, Y. Zeng, Fabrication and modeling of SiGe and Ge nanowires on insulator by three-dimensional Ge condensation method, *Semicond. Sci. Technol.* 34 (12) (2019) 125005.
- [20] D.E. Savage, J. Kleiner, N. Schimke, Y.H. Phang, T. Jankowski, J. Jacobs, R. Kariotis, M.G. Lagally, Determination of roughness correlations in multilayer films for x-ray mirrors, *J. Appl. Phys.* 69 (3) (1991) 1411–1424.
- [21] J.C. Tsang, P.M. Mooney, F. Dacol, J.O. Chu, Measurements of alloy composition

- and strain in thin $\text{Ge}_x\text{Si}_{1-x}$ layers, *J. Appl. Phys.* 75 (12) (1994) 8098–8108.
- [22] Y. Zhang, K. Cai, C. Li, S. Chen, H. Lai, J. Kang, Strain relaxation in ultrathin SGOI substrates fabricated by multistep Ge condensation method, *J. Electrochem. Soc.* 156 (2) (2009) H115.
- [23] S.-H. Huang, C. Li, W.-F. Lu, C. Wang, G.-Y. Lin, H.-K. Lai, S.-Y. Chen, Non-homogeneous SiGe-on-insulator formed by germanium condensation process, *Chin. Phys. B* 23 (4) (2014), 048109.
- [24] P.M. Mooney, F.H. Dacol, J.C. Tsang, J.O. Chu, Raman scattering analysis of relaxed $\text{Ge}_x\text{Si}_{1-x}$ alloy layers, *Appl. Phys. Lett.* 62 (17) (1993) 2069–2071.
- [25] Y. Chen, C. Li, H. Lai, S. Chen, Quantum-confined direct band transitions in tensile strained Ge/SiGe quantum wells on silicon substrates, *Nanotechnology* 21 (11) (2010) 115207.
- [26] H. Windischmann, Intrinsic stress in sputter-deposited thin films, *Crit. Rev. Solid State Mater. Sci.* 17 (6) (1992) 547–596.
- [27] Y. Okada, Y. Tokumaru, Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K, *J. Appl. Phys.* 56 (2) (1984) 314–320.
- [28] D.D. Cannon, J. Liu, Y. Ishikawa, K. Wada, D.T. Danielson, S. Jongthammanurak, J. Michel, L.C. Kimerling, Tensile strained epitaxial Ge films on Si(100) substrates with potential application in L-band telecommunications, *Appl. Phys. Lett.* 84 (6) (2004) 906–908.
- [29] J.-H. Zhao, T. Ryan, P.S. Ho, A.J. McKerrow, W.-Y. Shih, Measurement of elastic modulus, Poisson ratio, and coefficient of thermal expansion of on-wafer submicron films, *J. Appl. Phys.* 85 (9) (1999) 6421–6424.
- [30] J. Ma, Z. Fu, P. Liu, H. Zhang, Hole mobility enhancement in uniaxial stressed Ge dependence on stress and transport direction, *Sci. China Phys. Mech. Astron.* 57 (10) (2014) 1860–1865.
- [31] F. Murphy-Armando, S. Fahy, Giant enhancement of n-type carrier mobility in highly strained germanium nanostructures, *J. Appl. Phys.* 109 (11) (2011) 113703.
- [32] D. Nam, D.S. Sukhdeo, J.-H. Kang, J. Petykiewicz, J.H. Lee, W.S. Jung, J. Vučković, M.L. Brongersma, K.C. Saraswat, Strain-induced pseudoheterostructure nanowires confining carriers at room temperature with nanoscale-tunable band profiles, *Nano Lett.* 13 (7) (2013) 3118–3123.
- [33] P.E. Hellberg, S.L. Zhang, F.M. d'Heurle, C.S. Petersson, Oxidation of silicon–germanium alloys. I. An experimental study, *J. Appl. Phys.* 82 (11) (1997) 5773–5778.
- [34] V.L. Rideout, A review of the theory and technology for ohmic contacts to group III–V compound semiconductors, *Solid State Electron.* 18 (6) (1975) 541–550.
- [35] S. Averine, Y.C. Chan, Y.L. Lam, Evaluation of Schottky contact parameters in metal–semiconductor–metal photodiode structures, *Appl. Phys. Lett.* 77 (2) (2000) 274–276.
- [36] K. Mayes, A. Yasan, R. McClintock, D. Shiell, S.R. Darvish, P. Kung, M. Razeghi, High-power 280 nm AlGaIn light-emitting diodes based on an asymmetric single-quantum well, *Appl. Phys. Lett.* 84 (7) (2004) 1046–1048.
- [37] A. Dimoulas, P. Tsipas, A. Sotiropoulos, E.K. Evangelou, Fermi-level pinning and charge neutrality level in germanium, *Appl. Phys. Lett.* 89 (25) (2006) 252110.
- [38] G. Lin, M. Tang, C. Li, S. Huang, W. Lu, C. Wang, G. Yan, S. Chen, Formation of nickel germanide on SiO_2 -capped n-Ge to lower its Schottky barrier height, *Appl. Phys. Lett.* 103 (25) (2013) 253506.
- [39] M.M.A. Hakim, M. Lombardini, K. Sun, F. Giustiniano, P.L. Roach, D.E. Davies, P.H. Howarth, M.R.R. de Planque, H. Morgan, P. Ashburn, Thin film polycrystalline silicon nanowire biosensors, *Nano Lett.* 12 (4) (2012) 1868–1872.
- [40] A. Luque, A. Marti, A.J. Nozik, Solar cells based on quantum dots: multiple exciton generation and intermediate bands, *MRS Bull.* 32 (3) (2011) 236–241.
- [41] B. Tian, X. Zheng, T.J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, C.M. Lieber, Coaxial silicon nanowires as solar cells and nanoelectronic power sources, *Nature* 449 (7164) (2007) 885–889.